REMARKS

Applicants appreciate the thorough examination of the present application as evidenced by the Office Action of May 11, 2009 (hereinafter "Office Action"). Applicants have amended the claims as set out above and, therefore, respectfully submit that the pending claims are in condition for allowance for at least the reasons discussed herein.

The Section 102 Rejections

Claims 12-19 and 30 stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 5,583,362 to Maegawa (hereinafter "Maegawa"). *See* Office Action, page 3. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by Maegawa. For example, amended Claim 12 recites:

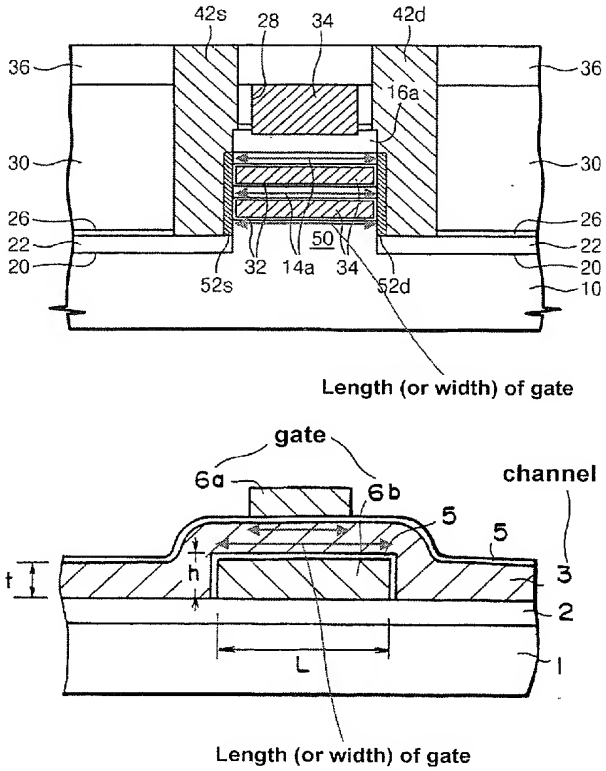
> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
>
> forming a MOS transistor on an integrated circuit substrate including an isolation layer and an active region higher than the isolation layer, the MOS transistor having a pair of junctions consisting of a vertical source region and a vertical drain region on the isolation layer, and a plurality of gates on the active region, **the plurality of gates being formed simultaneously to be stacked between the vertical source region and the vertical drain region;**
>
> forming a horizontal channel between the vertical source region and the vertical drain region **by growing single crystalline layers vertically spaced apart from each other on the active region, the channel including at least two horizontal channel regions formed in spaced apart patterns, wherein widths of the plurality of gates that contact the at least two horizontal channel regions are substantially identical, and** wherein the pair of junctions are vertically formed to cover the sides of the active region in other patterns adjacent to sides of the spaced apart patterns so that the pair of vertical junctions contact the sides of the at least two spaced apart horizontal channel regions; and
>
> forming a vertical source electrode electrically connected to the vertical source region and a vertical drain electrode electrically connected to the vertical drain region, wherein the vertical source and drain electrodes are formed on the isolation layer so that the vertical source and drain electrodes contact sides of the vertical source and drain regions, respectively.

Applicants respectfully submit that at least the highlighted recitations of amended independent Claim 12 are neither disclosed nor suggested by Maegawa for at least the reasons discussed herein.

The Office Action points to Figure 30, layers 22, 23, 25, 26, 27... as teaching the plurality of gates recited in Claim 12. *See* Office Action, page 4. As discussed in Maegawa,

these layers are formed serially. In stark contrast, amended Claim 12 recites "the plurality of gates being formed **simultaneously** to be stacked between the vertical source region and the vertical drain region." Accordingly, Applicants respectfully submit that amended independent Claim 12 and the claims that depend therefrom are patentable over Maegawa for at least the reasons discussed herein.

Furthermore, Claim 12 has been amended to recite that the "widths of the plurality of gates that contact the at least two horizontal channel regions are substantially identical." This aspect of the present invention is illustrated in the figure of the present application set out below. In stark contrast, as illustrated in Figure 15 of Maegawa set out below, the widths of gates are different which may adversely effect on electrical characteristics of the device. Accordingly, Applicants respectfully submit that independent Claim 12 and the claims that depend therefrom are patentable over the cited references for at least these reasons.



As discussed above, the dependent claims are patentable over the cited references for at least per the patentability of the independent base claims from which they depend. However, many of the dependent claims are also separately patentable. For example, amended dependent Claim 15 recites:

> The method of Claim 14, wherein the mask pattern is directly on the second epitaxial pattern, **the mask pattern preventing the plurality of gates from connecting to the vertical source and drain electrodes**.

As illustrated in the figure of the present application set out above, the mask pattern 16a prevents the gates 34 from contacting the vertical source/drain electrodes 42s/d. Nothing in Maegawa discloses or suggests preventing gates from contacting electrodes. Accordingly, Applicants respectfully submit that dependent Claim 15 is separately patentable over the cited references for at least these additional reasons.

Amended independent Claim 30 recites:

> A method of forming a unit cell of a metal oxide semiconductor (MOS) transistor, comprising:
>
> **providing an integrated circuit substrate including a trench and an active region higher than the trench, wherein the active region protrudes from the integrated circuit substrate to function as a horizontal channel;**
>
> forming the horizontal channel between a vertical source region and a vertical drain region , **the horizontal channel including at least two single crystalline horizontal channel regions formed in spaced apart patterns, and further including the active region higher than the trench**;
>
> **forming a plurality of gates simultaneously between at least two single crystalline horizontal channel regions, wherein widths of the plurality of gates that contact the at least two single crystalline horizontal channel regions are substantially identical;**
>
> forming the vertical source region and the vertical drain region in other patterns at one side of the spaced apart patterns, respectively, wherein the vertical source and drain regions extend along sides of the at least two horizontal channel regions and sides of the active region protruding from the integrated circuit substrate; and
>
> forming a vertical source electrode contacted to a side of the vertical source region and a vertical drain electrode contacted to a side of the vertical drain region.

Applicants respectfully submit that the highlighted portions of independent Claim 30 are patentable over Maegawa for at least reasons similar to those discussed above with respect to Claim 12.

Furthermore, independent Claim 30 has been amended to recite "providing an integrated circuit substrate including a trench and an active region higher than the trench, wherein the active region protrudes from the integrated circuit substrate to function as a horizontal channel." Nothing in the cited references discloses or suggests at least these additional recitations of independent Claim 30.

The Section 103 Rejections

Claims 20-29 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Maegawa in further view of United States Patent No. 6,420,758 to Nakajima (hereinafter "Nakajima"). *See* Office Action, page 7. Applicants respectfully submit that many of the recitations of these claims are neither disclosed nor suggested by the cited combination. For example, amended Claim 23 recites:

> A method of fabricating a transistor comprising:
> alternately stacking sets of first and second epitaxial layers on an integrated circuit substrate; and
> patterning the sets of the first and second epitaxial layers and the integrated circuit substrate to form a trench region on the integrated circuit substrate to define an active region, and a stacked structure including the sets of the first and second epitaxial patterns;
> forming a first insulation pattern on a floor of the trench;
> **growing a third epitaxial layer on sidewalls of the sets of first and second epitaxial patterns and sidewalls of the active region higher than the first insulation pattern**;
> forming a second insulation pattern on a surface of the integrated circuit substrate, the second insulation pattern defining a gate opening that exposes at least a portion of the third epitaxial layer;
> removing the third epitaxial layer in the gate opening to expose the sets of first and second epitaxial patterns;
> **selectively etching the first epitaxial patterns of the sets of first and second epitaxial patterns to form a horizontal channel region having a plurality of spaced apart single crystalline channel layers**;
> forming a gate oxide layer on a surface of channel layers;
> forming a gate pattern on the horizontal channel and in gap regions between the channel layers and the gate opening, **wherein the gate pattern comprises a plurality of gates formed simultaneously between the plurality of spaced apart single crystalline channel layers and widths of the plurality of gates that contact to the plurality of single crystalline channel layers are substantially identical**; and
> forming a vertical source electrode and a vertical drain electrode on the first insulation pattern penetrating the second insulation pattern to be connected to the third epitaxial layer.

Applicants respectfully submit that at least the highlighted recitations of amended independent Claim 23 are neither disclosed nor suggested by the cited combination for at least the reasons discussed herein.

The Office Action admits that Maegawa does not explicitly disclose the source/drain electrodes connected to the vertical source/drain regions. *See* Office Action, page 8. However, the Office Action states that it is notoriously well known to extend source/drain electrodes to make electrical contact with the source/drain regions and points to Nakajima as teaching source/drain electrodes to the source/drain regions. The Office Action concludes that the combination of Maegawa and Nakajima would show the vertical source/drain electrodes connected to the vertical source/drain regions as recited in Claim 23. Applicants respectfully disagree.

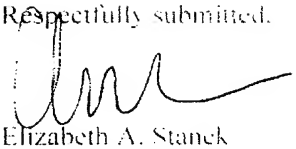
Applicants have amended Claim 23 to recite formation of single crystalline horizontal channels by epitaxial growth of Si (second epitaxial layer) on Si or SiGe layer (first epitaxial layer). Single crystalline Si can be formed on Si or SiGe. In stark contrast, Maegawa discloses formation of Si channels on an oxide film 2 and a nitride film 8. *See e.g.*, Figure 1B of Maegawa. It may be difficult to form a single crystalline Si layer on the insulation layer. For this reason, Maegawa discloses the formation of Si channel by deposition of polysilicon as discussed, for example, at column 6, lines 17~ 22. Accordingly, Applicants respectfully submit that independent Claim 23 and the claims that depend therefrom are patentable over the cited combination for at least these reasons.

Furthermore, mobility of electrons in the single crystalline Si is higher, for example, 2 ~ 10 times higher, than in the poly crystalline Si. Therefore, electrical characteristics of devices according to some embodiments of the present invention may have a higher electron mobility than devices of Maegawa.

CONCLUSION

Applicants respectfully submit that pending claims are in condition for allowance, which is respectfully requested in due course. Favorable reconsideration of this application is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

Respectfully submitted,



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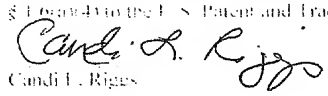

Candi L. Riggs